IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: BUR9200000199
William D. Corti	
Serial No.: 09/683,091	Group Art Unit: 2184
Confirmation No.: 8058	
Filed: November 16, 2001	Examiner: Wilson, Yolanda L.

For: **ON-CHIP LOGIC ANALYZER**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. § 1.131

Sir:

We, Steven C. Parker, Joseph O. Marsh, Robert Kenny, Jr., Michael Won, William D. Corti and Frank X. Scanzano, do hereby declare:

1. We are co-inventors of the subject matter disclosed and recited in independent claims 1, 17, and 19 of the above-identified application.

2. We completed the invention of claims 1, 17 and 19 (and those claims dependent thereon) in the United States before March 26, 2001, as evidenced below.

CONCEPTION

3. Before March 26, 2001 we conceived of an on-chip logic analysis system including a single chip device including a signal processing unit and a host unit externally provided as disclosed and recited in independent claims 1, 17 and 19 of the application, of which

is evidenced by IBM Disclosure BUR-2000-0250 (hereinafter referred to as "the Invention Disclosure") attached hereto as Exhibit A. The Invention Disclosure attached hereto is a photocopy of and is identical to the originals, except that all pertinent dates have been removed therefrom.

4. All pertinent dates removed from the Invention Disclosure attached hereto are before March 26, 2001.

5. As evidenced in the Invention Disclosure, the on-chip logic analysis (OCLA) system includes:

a. a single chip device (e.g., DSP core logic) including a signal processing unit, a plurality of memory blocks, and a data capturing unit;

b. a host unit externally provided to said single chip device and generating control signals to control the data capturing unit; and

c. the data capturing unit captures data processed by the signal processing unit in response to the control signals from the host unit and transfers the captured data to the host without interrupting operations of the signal processing unit.

6. In further embodiments, as evidenced in the Invention Disclosure, the on-chip logic analysis system also includes, for example:

a. an OCLA unit capturing data processed by the signal processing unit in response to the control signals from the host unit and transfers the captured data to the host without interrupting operations of the signal processing unit; and

b. a DSP core logic.

7. The benefits and features of the on-chip logic analyzer are shown and described in

the Invention Disclosure and accompanying documents.

8. These features and others are exemplified in the figures in the Invention Disclosure.

DUE DILIGENCE

9. Prior to March 26, 2001, the inventors submitted the Invention Disclosure to IBM counsel for review and preparation of a patent application.

10. Prior to the filing of the present application in the U.S. Patent Office, Inventor Parker communicated with patent counsel at McGuireWoods LLP, on behalf of all of the inventors, in preparing a patent application based on the Invention Disclosure. For example, communications took place on July 9 and 19, 2001, August 23, 2001 and up to and including correspondences dated November 7, 2001.

11. During this time and prior to March 26, 2001, we worked diligently on providing information to IBM in house counsel and preparing the patent application for filing in the U.S. Patent Office. All of the inventors were involved in reviewing and finalizing the application for the present invention prior to the filing of the above-identified application.

12. We worked diligently on the preparation of the patent application with patent counsel at McGuireWoods until a final draft patent application was completed to our satisfaction. A final draft of the application was forwarded to us by IBM in-house attorney, Richard Henkler, who received the final draft from then McGuireWoods attorney Kevin Reif in a letter dated November 13, 2001. At all times, we worked diligently to finalize the application for filing in the U.S. Patent and Trademark Office from prior to March 26, 2001 to the finalized application on November 13, 2001.

13. The patent application was filed in the U.S. Patent and Trademark Office on November 16, 2001.

14. We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Steven C. Parker — Date: 10/17/2003

Joseph O. Marsh — Date: 10/17/2003

Robert Kenny, Jr. — Date

Michael Won — Date: 10/17/2003

William Corti — Date: 10/17/2003

Frank X. Scanzano — Date

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